|  |
| --- |
|  |
|  |  | **1 -------------------------------------------------------**  **2 -- Design Name : pri\_encoder\_using\_if**  **3 -- File Name : pri\_encoder\_using\_if.vhd**  **4 -- Function : Pri Encoder using If**  **5 -- Coder : Deepak Kumar Tala (Verilog)**  **6 -- Translator : Alexander H Pham (VHDL)**  **7 -------------------------------------------------------**  **8 library ieee;**  **9 use ieee.std\_logic\_1164.all;**  **10**  **11 entity pri\_encoder\_using\_if is**  **12 port (**  **13 enable :in std\_logic; -- Enable for the encoder**  **14 encoder\_in :in std\_logic\_vector (15 downto 0);-- 16-bit Input**  **15 binary\_out :out std\_logic\_vector (3 downto 0) -- 4 bit binary Output**  **16**  **17 );**  **18 end entity;**  **19**  **20 architecture behavior of pri\_encoder\_using\_if is**  **21**  **22 begin**  **23 process (enable, encoder\_in) begin**  **24 binary\_out <= "0000";**  **25 if (enable = '1') then**  **26 if (encoder\_in = "XXXXXXXXXXXXXX10") then**  **27 binary\_out <= "0001";**  **28 elsif (encoder\_in = "XXXXXXXXXXXXX100") then**  **29 binary\_out <= "0010";**  **30 elsif (encoder\_in = "XXXXXXXXXXXX1000") then**  **31 binary\_out <= "0011";**  **32 elsif (encoder\_in = "XXXXXXXXXXX10000") then**  **33 binary\_out <= "0100";**  **34 elsif (encoder\_in = "XXXXXXXXXX100000") then**  **35 binary\_out <= "0101";**  **36 elsif (encoder\_in = "XXXXXXXXX1000000") then**  **37 binary\_out <= "0110";**  **38 elsif (encoder\_in = "XXXXXXXX10000000") then**  **39 binary\_out <= "0111";**  **40 elsif (encoder\_in = "XXXXXXX100000000") then**  **41 binary\_out <= "1000";**  **42 elsif (encoder\_in = "XXXXXX1000000000") then**  **43 binary\_out <= "1001";**  **44 elsif (encoder\_in = "XXXXX10000000000") then**  **45 binary\_out <= "1010";**  **46 elsif (encoder\_in = "XXXX100000000000") then**  **47 binary\_out <= "1011";**  **48 elsif (encoder\_in = "XXX1000000000000") then**  **49 binary\_out <= "1100";**  **50 elsif (encoder\_in = "XX10000000000000") then**  **51 binary\_out <= "1101";**  **52 elsif (encoder\_in = "X100000000000000") then**  **53 binary\_out <= "1110";**  **54 else**  **55 binary\_out <= "1111";**  **56 end if;**  **57 end if;**  **58 end process;**  **59 end architecture;**  You could download file vhdl\_examples [here](http://www.asic-world.com/code/vhdl_examples/pri_encoder_using_if.vhd) |
|  |  |  |
|  |  | **Encoder - Using when Statement** |
|  |  |  |
|  |  | **1 -------------------------------------------------------**  **2 -- Design Name : pri\_encoder\_using\_when**  **3 -- File Name : pri\_encoder\_using\_when.vhd**  **4 -- Function : Pri Encoder using when-else**  **5 -- Coder : Deepak Kumar Tala (Verilog)**  **6 -- Translator : Alexander H Pham (VHDL)**  **7 -- Fixed : Tomasz Olszewski**  **8 -------------------------------------------------------**  **9 library ieee;**  **10 use ieee.std\_logic\_1164.all;**  **11**  **12 entity pri\_encoder\_using\_when is**  **13 port (**  **14 enable :in std\_logic; -- Enable for the encoder**  **15 encoder\_in :in std\_logic\_vector (15 downto 0);-- 16-bit Input**  **16 binary\_out :out std\_logic\_vector (3 downto 0) -- 4 bit binary Output**  **17**  **18 );**  **19 end entity;**  **20**  **21 architecture behavior of pri\_encoder\_using\_when is**  **22**  **23 begin**  **24 binary\_out <= "0000" when enable = '0' else**  **25 "0001" when encoder\_in( 1 ) = '1' else**  **26 "0010" when encoder\_in( 2 ) = '1' else**  **27 "0011" when encoder\_in( 3 ) = '1' else**  **28 "0100" when encoder\_in( 4 ) = '1' else**  **29 "0101" when encoder\_in( 5 ) = '1' else**  **30 "0110" when encoder\_in( 6 ) = '1' else**  **31 "0111" when encoder\_in( 7 ) = '1' else**  **32 "1000" when encoder\_in( 8 ) = '1' else**  **33 "1001" when encoder\_in( 9 ) = '1' else**  **34 "1010" when encoder\_in( 10 ) = '1' else**  **35 "1011" when encoder\_in( 11 ) = '1' else**  **36 "1100" when encoder\_in( 12 ) = '1' else**  **37 "1101" when encoder\_in( 13 ) = '1' else**  **38 "1110" when encoder\_in( 14 ) = '1' else**  **39 "1111" when encoder\_in( 15 ) = '1' else**  **40 "0000";**  **41**  **42 end architecture;** |

**VHDL Code -**  
  
  
  
-------------------------------------------------------------------------------  
--  
-- Title       : priority\_encoder\_8\_3  
-- Design      : vhdl\_upload2  
-- Author      : Naresh Singh Dobal  
-- Company     : nsdobal@gmail.com  
-- Verilog HDL Programs &  Exercise with Naresh Singh Dobal.  
--  
-------------------------------------------------------------------------------  
--  
-- File        : Design of Priority Encoder using if else statements.vhd  
  
      
  
library IEEE;  
use IEEE.STD\_LOGIC\_1164.all;        
use ieee.numeric\_std.all;  
  
entity priority\_encoder\_8\_3 is  
     port(  
         din : in STD\_LOGIC\_VECTOR(7 downto 0);  
         dout : out STD\_LOGIC\_VECTOR(2 downto 0)  
         );  
end priority\_encoder\_8\_3;  
  
  
architecture priority\_enc\_arc of priority\_encoder\_8\_3 is  
begin  
  
    pri\_enc : process (din) is  
    begin  
        if (din(7)='1') then  
            dout <= "000";  
        elsif (din(6)='1') then  
            dout <= "001";  
        elsif (din(5)='1') then  
            dout <= "010";  
        elsif (din(4)='1') then  
            dout <= "011";  
        elsif (din(3)='1') then  
            dout <= "100";  
        elsif (din(2)='1') then  
            dout <= "101";  
        elsif (din(1)='1') then  
            dout <= "110";  
        elsif (din(0)='1') then  
            dout <= "111";  
        end if;  
    end process pri\_enc;  
      
  
end priority\_enc\_arc;